a register which stores a value which is representative of a delay time after which the memory device responds to a read request; and

a plurality of output drivers to output data in accordance with the delay time and synchronously with respect to the external clock signal.

152. The memory device of claim 151 further including:

clock generation circuitry, coupled to the clock receiver circuitry, to generate at least one internal clock signal; and

wherein the plurality of output drivers output data in response to the internal clock signal.

153. The memory device of claim 152 wherein the plurality of output drivers output data in response to a rising edge of the internal clock signal.

154. The memory device of claim 151 further including:

a delay locked loop, coupled to the clock receiver circuitry, to generate an internal clock signal using at least the external clock signal; and

wherein the plurality of output drivers output data in response to the internal clock signal.

155. The memory device of claim 151 wherein the value which is representative of the delay time is stored in the register after power is applied to the device.

156. The memory device of claim 151 wherein the value stored in the register is representative of one of a plurality of different delay times.

157. A synchronous semiconductor memory device having at least one memory section including a plurality of memory cells, the memory device comprising:

clock receiver circuitry to receive an external clock signal;

at least one register to store a value which is representative of a delay time; and

wherein in response to a read request, the memory device outputs data in accordance with the delay time and synchronously with respect to the external clock signal.

158. The memory device of claim 157 further including:

clock generation circuitry, coupled to the clock receiver circuitry, to generate an internal clock signal; and

an output driver, coupled to the internal clock generation circuitry, to output the data in response to the internal clock signal.

159. The memory device of claim 158 wherein the output driver outputs data in response to a rising edge of the internal clock signal.

160. The memory device of claim 157 further including a delay locked loop, coupled to the clock receiver circuitry, to generate

an internal clock signal using at least the external clock signal and wherein the output driver outputs data in response to the internal clock signal.

161. The memory device of claim 157 wherein the memory device, in response to a set register request, stores a value in the at least one register.

162. The memory device of claim 157 wherein the value stored in the register is representative of one of a plurality of available delay times.

163. A method of operating a synchronous semiconductor memory device having at least one memory section including a plurality of memory cells and a register for storing a value which is representative of a time delay after which the memory device responds to a read request, the method comprising:

issuing a read request to the memory device wherein the memory device, in response to the read request, outputs data on a bus in accordance with the time delay and synchronously with respect to an external clock signal.

164. The method of claim 163 further including issuing a set register request, wherein, in response to the set register request, the memory device stores the value in the register.

165. The method of claim 164 wherein the set register request and the value are provided to the memory device in a single request packet.

166. The method of claim 163 wherein the read request and information identifying the time delay after which the memory device responds to a read request are provided to the memory device in a single request packet.

167. The method of claim 163 further including the steps of:

initializing the register in the memory device by issuing a set register request on the bus; and

providing the value which is representative of the time delay.

168. The method of claim 163 further including the step of identifying the memory device on the bus using a device identification code.

169. The method of claim 168 wherein the device identification code and information identifying the time delay after which the memory device responds to a read request are provided to the memory device in a single request packet.

170. The method of claim 168 wherein the device identification code is a unique device code.